What is claimed is:

1. A method of fabricating a double diffused MOS (DMOS) transistor structure, the method comprising:

forming an epitaxial silicon layer having a first conductivity type on a silicon substrade;

forming a well region having a second conductivity type that is opposite the first conductivity type in the epitaxial silicon layer;

forming a dielectric isolation region in the epitaxial silicon layer at the periphery of the well region;

forming a trench trough in the epitaxial silicon layer such that one of the walls of the trench trough comprises exposed epitaxial silicon and remaining walls of the trench trough comprise dielectric isolation material;

performing a trench trough implant to introduce dopant of the second conductivity type into the epitaxial silicon layer under the trench trough to form a connection region having the second conductivity type that extends into contact with the well region and introduces dopant of the second conductivity type into the epitaxial silicon sidewall of the trench trough;

forming a gate dielectric layer on exposed sidewalls of the trench trough;

forming a conductive layer on the gate dielectric layer;

etching the conductive layer to define a conductive gate electrode of the DMOS transistor structure;

performing a body implant to introduce dopant of the first conductivity type on one side of the conductive gate electrode to form a body implant region having the first conductivity type in the epitaxial silicon layer;

forming dielectric sidewall spaces on sidewalls of the conductive gate electrode;

forming a contact region having the first conductivity type in the body implant region; and

forming source and drain regions having the second conductivity type in the epitaxial silicon layer.

2. A method as in claim 1, and wherein the body implant region is spaced-apart from the connection region.

3. A method of fabricating a double diffused MOS (DMOS) transistor structure, the method comprising:

forming a P-type epitaxial silicon layer on a P-type silicon substrate;

forming a N-type well region in the epitaxial silicon layer;

forming a dielectric isolation region in the epitaxial silicon layer at the periphery of the N-type well region;

forming a trench trough in the epitaxial layer such that one of the walls of the trench trough comprises exposed epitaxial silicon and remaining walls of the trench trough comprise dielectric isolation material;

performing a trench trough implant to introduce N-type dopant into the epitaxial layer under the trench trough to form a N-type connection region that extends into contact with the N-well region and introduces N-type dopant into the epitaxial silicon sidewall of the trench trough;

forming a layer of gate oxide on exposed sidewalls of the trench trough;

forming a layer of polysilicon on the gate oxide layer;

etching the polysilicon layer and the gate oxide layer to define a polysilicon gate electrode of the DMOS transistor structure;

performing a P-body implant to introduce P-type dopant on one side of the polysilicon gate electrode to form a P-body implant region in the epitaxial silicon layer;

forming silicon oxide sidewall spacers on sidewalls of the polysilicon gate electrode; and

forming a P+ region and N+ source/drain regions in the epitaxial silicon layer.

4. A method as in claim 3, and wherein the P-body implant region and the N-type connection region are spaced-apart.

5. A double diffused MOS (DMOS) transistor structure comprising:

an epitaxial silicon layer having a first conductivity type formed on a silicon substrate;

a well region having a second conductivity type that is opposite the first conductivity type formed in the epitaxial silicon layer;

a dielectric isolation region formed in the epitaxial silicon layer at the periphery of the well region;

a trench trough formed in the epitaxial silicon layer such that one of the walls of the trench trough comprises exposed epitaxial silicon and remaining walls of the trench trough comprise dielectric isolation material;

a connection region having the second conductivity type formed in the epitaxial silicon layer under the trench trough, and extending into contact with the well region, and comprising dopant of the second conductivity type introduced into the epitaxial silicon sidewall of the trench trough;

a conductive gate electrode formed to extend into the trench trough but to be separated from sidewalls of the trench trough by intervening gate dielectric material; and

a body implant region having the first conductivity type formed in the epitaxial silicon layer on one side of the conductive gate electrode.

6. A double diffused MOS (DMOS) transistor structure as in claim 5, and wherein the body implant region is spaced-apart from the connection region.